QUASI-OPTICAL WATT-LEVEL MILLIMETER-WAVE MONOLITHIC SOLID-STATE DIODE-GRID FREQUENCY MULTIPLIERS

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ABSTRACT

A monolithic planar array containing thousands of GaAs Barrier-Intrinsic-N^+ (BIN) diodes have produced one watt output power at 100 GHz in a tripler configuration in excellent agreement with the predictions from large-signal nonlinear circuit analysis of frequency multiplication. Significant improvement is expected with realizable diode parameters and optimized pumping condition.

INTRODUCTION

Inexpensive watt level CW solid-state sources are required for a variety of millimeter and submillimeter wave applications. Available solid-state oscillators, such as GaAs Gunn diodes and IMPATTs, are highly efficient and tunable, but are currently limited to frequencies up to about 75 GHz and 150 GHz, respectively. Much higher frequencies can be obtained by generating harmonics of the fundamental frequency from solid-state oscillators operating at a lower frequency. This motivated our design of a diode grid for frequency multiplication. The approach [2] is attractive because a grid is monolithically integrated with thousands of diodes thereby resulting in potentially low-cost fabrication and small-size realization. It overcomes the power limitations of a single-diode multiplier because power is distributed among many diodes making possible watt level output power throughout the millimeter wave region.

BACKGROUND

Monolithic Schottky diode grids have been fabricated on 2-cm square GaAs wafers in a proof-of-principle test of the quasi-optical millimeter-wave varactor diode frequency multiplier array concept [4]. A doubling efficiency of 9.5% and output power of 0.5 W was achieved at 66 GHz when the diode grid was pumped with a pulsed source at 33 GHz. Futhermore, the diode-grid equivalent circuit model based on a transmission line analysis of plane wave illumination has been verified experimentally over a frequency range from 33 GHz to 140 GHz [5]. The equivalent circuit model together with a large-signal multiplier analysis [6] of the nonlinear varactor diode impedances were used to predict the doubler performance and to facilitate detailed comparison between theory and experiment.

In parallel with the GaAs Schottky diode doubler array studies, we investigated the use of a MOS structure having an undoped epitaxial layer, which is grown on a heavily doped substrate and isolated by a thin oxide layer [7]. The space-charge-limited current which is injected into the epilayer from the heavily doped substrate produces a step-like capacitance-voltage characteristic resulting in increased harmonic generation efficiency. The thin MOS concept was tested by used honeycomb arrays which were mounted in crossed waveguide mounts and whisker contacted. The experimental results show good agreement with the analytical predictions [1,8] and the large-signal multiplier analysis [6]. A maximum efficiency of 17% was predicted for the 2 μm radius device which is in good agreement with the 14.7% obtained experimentally.

Another important feature of these devices is that, due to the blocking barrier, two diodes can be operated back-to-back generating a sharp spike in the capacitance-voltage curve. The height and width of this capacitance-voltage characteristic can, in principle, be adjusted by doping control alone thus eliminating the need for an external dc bias. This arrangement needs no external ohmic contact resulting in a highly efficient frequency tripler. However, defects in the epitaxial silicon layer deteriorated the thin oxide and limited the yield of the devices making array construction difficult.

BARRIER-INTRINSIC-N^+ DIODE TRIPLER ARRAY

Device Concept

Recently, a GaAs barrier-intrinsic-N^+ (BIN) diode has been described [7] as shown in Fig. 1. This structure eliminates the problem of low fabrication yield associated with the thin MOS structure and takes advantage of the higher mobility of GaAs. It does not require an insulating layer as in the thin MOS structure but, instead, relies on a Mott-type barrier formed between the metal gate and a sheet of positive charge created by a thin heavily doped n^+ region in the GaAs. The maximum cut-off frequency is

determined by the time it takes electrons to transit the space charge layer at saturation velocity. As with the MOS diode, the blocking barrier permits a back-to-back fabrication arrangement which results in a highly efficient tripler operation. The initial BIN diode structure was grown with a conservative fabrication design (1500 Å thick epitaxial layer). This gives an intrinsic cut-off frequency of 640 GHz.

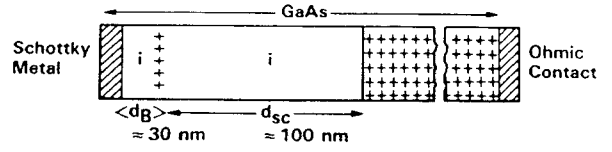

Fig. 1 Structure of the GaAs BIN diode.

Metal-Grid Design

The metal grid we have designed for the BIN diode tripler consists of a columnar mesh of metal strips with Schottky electrodes on each end as shown in Fig. 2. The period of the grid is chosen to be about half the dielectric wavelength to avoid exciting substrate modes. A reasonable grid inductance is then achieved by choosing the strip width of 20 μm. The small dimensions and rectangular shape of the Schottky electrode are designed to minimize the zero-voltage capacitance and series resistance of the device, respectively. This arrangement leads to a high cut-off frequency of the BIN diode. The two neighboring Schottky electrodes are designed to provide the back-to-back configuration for two BIN diodes. The design requires only one metal pattern, which greatly facilitates the fabrication. The symmetrical capacitance-voltage curve measured from two back-to-back connected BIN diodes illustrated in Fig. 3 demonstrates the concept of the back-to-back configuration for highly efficient frequency tripler operation.

Large-Signal Nonlinear Circuit Analysis

In this work, we have extensively made use of the nonlinear analysis program [6] in order to estimate the performance of the BIN diode tripler employing the back-to-back configuration. The program has also been used to evaluate the importance of diode and embedding network parameters. In addition, an interpolation sub-program has been employed in the nonlinear analysis program in order to use the experimentally measured C-V data. The measured series resistance of 15 Ω is also used for the following computation cases.

The symmetric capacitance-voltage characteristics of two back-to-back connected GaAs BIN diodes result in cancellation of even harmonics. This can be seen from the large signal analysis results in Fig. 4, which shows that the efficiency is insensitive to second harmonic impedance. Therefore, the back-to-back configuration of two BIN diodes also favors tripler operation since there is no need for an even harmonic idler circuit in the diode-grid tripler configuration. This arrangement greatly simplifies the circuit design.

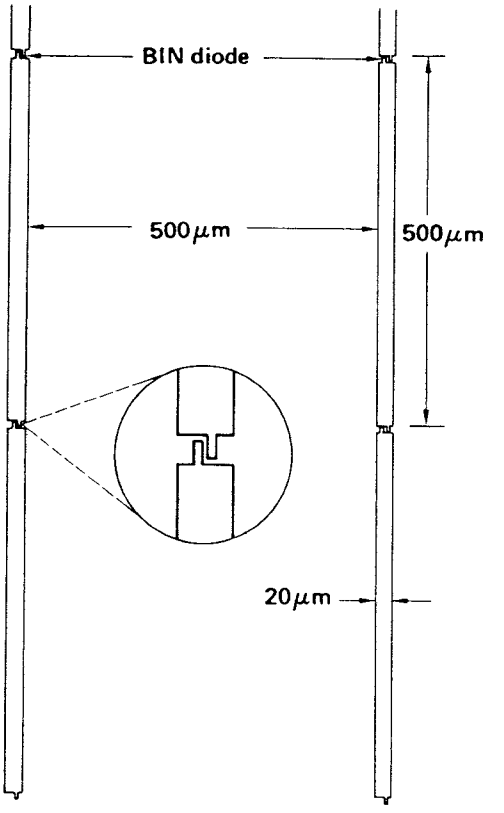

Fig. 2 Design of metal grid for the BIN diode tripler array.

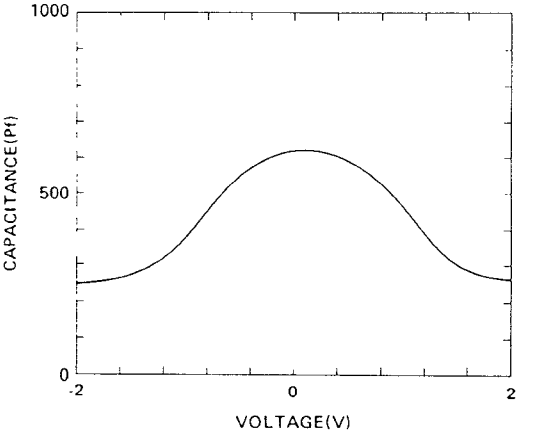

Fig. 3 Symmetrical capacitance-voltage characteristic from two back-to-back connected GaAs BIN diodes.

It should be mentioned that the input power is 10 mW for the above analysis study. Figure 5 shows the tripling efficiency versus input power level

for various input frequencies. The input and output tuning were optimized at each frequency. As shown in Fig. 5, the efficiency is highest with an input power level of ~ 10 mW. Over the output frequency range of 100-150 GHz, an efficiency greater than 15% is predicted using the parameters of the GaAs BIN array which has recently been fabricated. The highest efficiency is 24% at 100 Ghz obtained with an input power of 9.0 mW per diode, which shows excellent agreement with the analytical predictions [1,8].

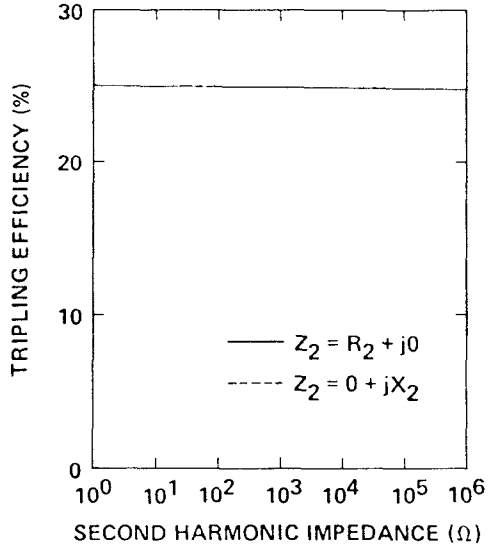

Fig. 4 Tripling efficiency versus second harmonic resistance and reactance.

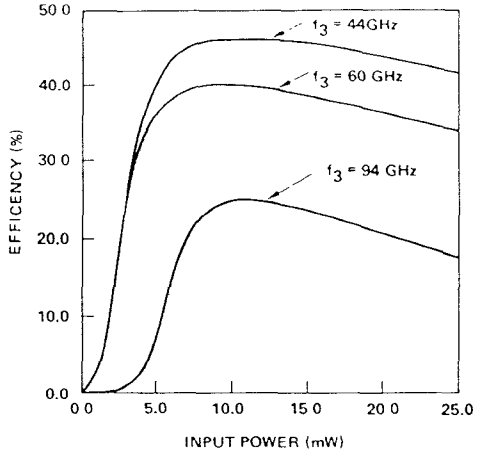

Fig. 5 Tripling efficiency versus input power at various input frequencies.

Substantial improvements are possible for the BIN diode. Recently, we have managed to increase the doping concentration of the back contact region to $6x10^{18}$ cm^{-3}. A series resistance of 5 Ω is achieved. Figure 6 shows the simulated tripling efficiency results as a function of the series resistance. The input and output impedances are the optimized values. The simulated results are in excellent agreement with the analytical values predicted in Ref [5,6]. The simulation result predicts a maximum tripling efficiency of 60% at an output frequency of 100 GHz for this recently fabricated BIN diode.

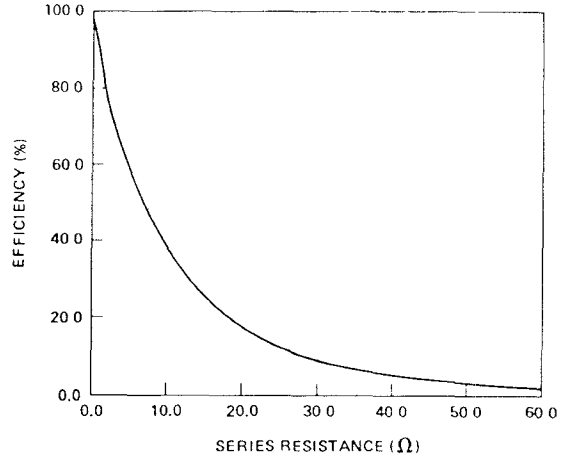

Fig. 6 Tripling efficiency versus diode series resistance.

Quasi-Optical Diode-Grid Tripler Configuration

A complete quasi-optical diode-grid tripler design has also been developed as shown in Fig. 7, where power at the fundamental frequency enters from the bottom, through an input tuner. The blazed grating plate (which functions as a high-pass transmission filter) reflects (as a mirror) the incident pump power at the fundamental frequency to the diode grid on the left of it, and the metal mirror behind the diode grid again reflects all the harmonics back to the grating plate. Different harmonics are then diffracted in different directions. The third harmonic is designed to exit in the desired direction passing through an output tuner. It should be recalled that, due to the elimination of even harmonics, even harmonic idler circuits are unnecessary in the diode-grid tripler design.

Device Performance

Using the quasi-optical diode-grid tripler configuration shown in Fig. 7 for a proof-of-principle test, a watt output power at an output frequency of 100 GHz with a tripling efficiency 8.5% has been experimentally obtained from approximately 4 mW incident power on each diode. This experimental measurement is in good agreement with the large-signal nonlinear circuit analysis

prediction (see Fig. 5). It should be mentioned that this preliminary result was performed in the low input power region. However, an optimized pumping operation promises increased performance.

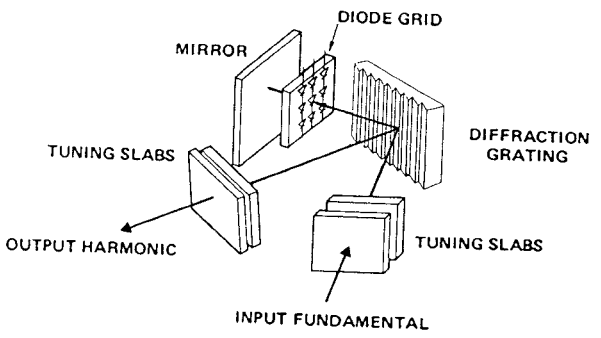

Fig. 7 Configuration of the diode-grid tripler.

SUMMARY AND CONCLUSION

A watt output power at 100 GHz has been obtained for the monolithic planar BIN diode-grid tripler array in the initial proof-of-principle study. The device performance is limited by the parameters of fabricated diodes. Significant improvement can be obtained with realizable diode parameters.

ACKNOWLEDGEMENT

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